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Interfacial Reaction and Electrical Properties of HfO_2 Film Gate Dielectric Prepared by Pulsed Laser Deposition in Nitrogen: Role of Rapid Thermal Annealing and Gate Electrode

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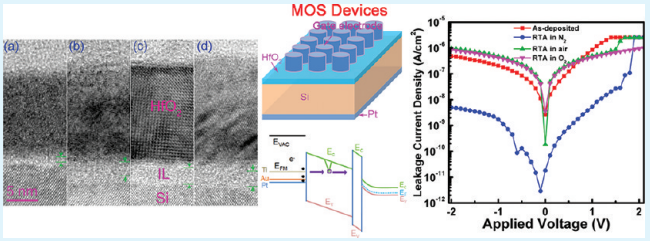
ABSTRACT: The high-k dielectric HfO_2 thin films were deposited by pulsed laser deposition in nitrogen atmosphere. Rapid thermal annealing effect on film surface roughness, structure and electrical properties of HfO_2 film was investigated. The mechanism of interfacial reaction and the annealing atmosphere effect on the interfacial layer thickness were discussed. The sample annealed in nitrogen shows an amorphous dominated structure and the lowest leakage current density. Capacitors with high-k HfO_2 film as gate dielectric were fabricated, using Pt, Au, and Ti as the top gate electrode whereas Pt constitutes the bottom side electrode. At the gate injection case, the Pt- and Au-gated metal oxide semiconductor devices present a lower leakage current than that of the Ti-gated device, as well as similar leakage current conduction mechanism and interfacial properties at the metal/HfO_2 interface, because of their close work function and chemical properties.



KEYWORDS: dielectric thin films, laser deposition, metal−insulator-semiconductor structures, conduction mechanism

1. INTRODUCTION

The continuous miniaturization of the metal oxide semiconductor field effect transistors (MOSFET) gate length, in order to realize high-performance ultra large scale integration (ULSI) circuits, has given the microelectronic industry new problems to overcome.[1,2] One of them is the corresponding scaling down of the gate oxide thickness; the silicon dioxide and silicon nitride are being scaled down to their physical limits. To overcome this serious problem, we will replace Si-based dielectrics by the so-called high-k materials,[1−3] which will maintain low leakage current, high breakdown voltage, and good performance. HfO_2 is a leading candidate among many high-k dielectrics because of its outstanding characteristics, including excellent thermodynamic stability, high dielectric constant, relatively wide band gap, and high breakdown electric field.[1,4,5] However, one drawback of HfO_2 is the low crystallization temperature, the reliability of the dielectric after postannealing is a crucial issue to be investigated. Generally, as-deposited HfO_2 is amorphous, it may form three crystalline phases at different temperatures: monoclinic (∼400 or 500 °C), tetragonal (∼1720 °C) and cubic (2600 °C).[1,3] Meanwhile, orthorhombic phase is also reported.[6] Furthermore, despite some efforts to fabricate devices with high-k dielectric and poly silicon gates,[7,8] most high-k dielectric are not compatible with the poly silicon gate electrode because of the interaction between the poly silicon gate electrode and the new high-k dielectrics.[1] Since direct metal gate on HfO_2 can provide good thermal stability and equivalent oxide thickness (EOT) scaling, the exploration of relevant metal gate materials for band edge threshold voltage tuning efforts kicked off very actively. Recently, many metals[9−12] as well as metal nitride[13,14] and metal silicide[15,16] have been investigated as top electrode for high-k dielectric. However, for the elemental metal gate most of them are performed on metal−insulator−metal, there is lack of information about metal gate effect on the electrical properties of HfO_2-based metal-oxide-semiconductor (MOS) capacitors.

In this work, MOS capacitors were fabricated, using pulsed laser deposited high-k HfO_2 thin film as gate dielectric. The changes in the surface morphology, structural, dielectric, and electrical properties of the HfO_2 gate dielectric thin films due to rapid thermal annealing (RTA) were investigated in detail.

2. EXPERIMENTAL SECTION

2.1. Preparation Process of HfO_2 Films and MOS Devices.

MOS capacitors with high-k HfO_2 thin film as gate dielectric were fabricated on p-Si wafers by pulsed laser deposition (PLD), using three different metals (Pt, Ti, Au) for the top gate electrode. First, a thin HfO_2 film was grown on the p-Si (100) wafer at room temperature from a HfO_2 ceramic target (purity 99.99%) with a target-substrate distance of 4 cm, using a KrF excimer pulsed laser (Lambda Physik, λ = 248 nm) operated at 4 Hz and energy of 150 mJ/pulse. Prior to deposition, the Si substrates were dipped into 10% HF solution for 30s to remove native oxide and then cleaned with acetone, anhydrous, and deionized water.

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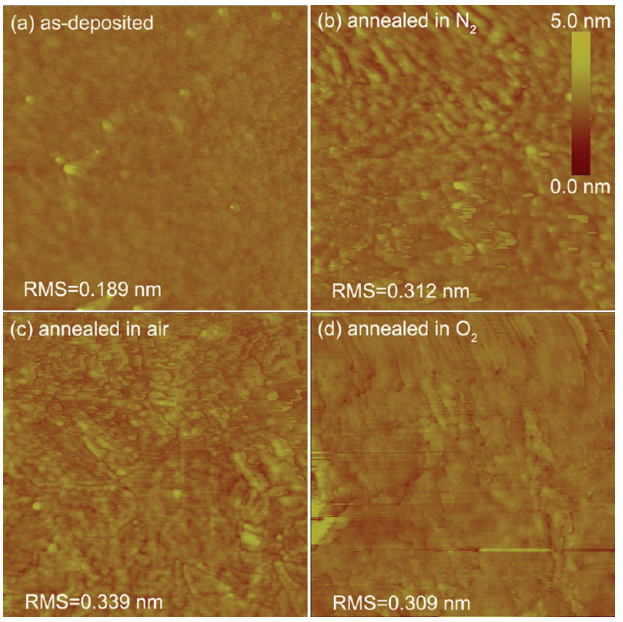

Figure 1. AFM images of the HfO_2 films for: (a) as-deposited and rapid thermal annealed in (b) N_2, (c) air, and (d) O_2; the scan size is 1 × 1 μm^2.

The chamber was pumped down to base pressure of ~2 × 10^{-6} Torr and we fixed the N_2 flux at 4 SLM and adjusted the valve of the pump to maintain the chamber pressure at 1.125 × 10^{-4} Torr. During film deposition, the target and substrate were continuously rotated to avoid the formation of craters. The as-deposited HfO_2 thin films were fallowed by a RTA step, in N_2, air and O_2 environment and at a temperature of T = 900 °C for 1 min. Second, MOS capacitors were fabricated. To avoid the influence from the back side electrode, all the MOS devices possess the same Pt back side electrode deposited by magnetron sputtering. And three different top metal electrodes, Pt, Ti, and Au, were deposited by sputtering on the as-deposited HfO_2 thin film through a shadow mask. The capacitor area was 1.96 × 10^{-7} m^2.

2.2. Characterization. The HfO_2 films roughness was measured by atomic force microscopy (AFM) in tapping mode, and the root-mean-square (rms) roughness values were calculated on 1 × 1 μm^2. The structure of the dielectric was analyzed by X-ray diffraction (XRD, Bruker D8) and the physical thickness of the dielectric layer was determined by cross-section high resolution transmission electron microscopy (HRTEM). The capacitance−voltage (C−V) and current−voltage (I−V) characteristics were measured by HP 4284A Precision LCR Meter and HP 4145B Semiconductor Parameter Analyzer, respectively. All the capacitance was measured at 10 kHz. All the electrical tests were carried out in a dark box and all the test equipments were interfaced with a computer and a switch matrix was used for automated testing.

3. RESULTS AND DISCUSSION

3.1. Surface and Interface Structure of HfO_2 Dielectric Layer. AFM was used to study the thermal treatment impact on the surface morphology of the HfO_2 films. Figure 1 shows AFM images of the as-deposited HfO_2 film and after RTA, respectively. The rms surface roughness of the HfO_2 films slightly increased after RTA treatment from 0.189 nm to 0.312 nm, 0.339 nm, and 0.309 nm, respectively. Obviously, an atomic level surface roughness which withstands annealing to 900 °C was achieved by PLD. The slight increase in surface roughness after RTA processing was due to crystallization and/or grain growth during annealing.[6]

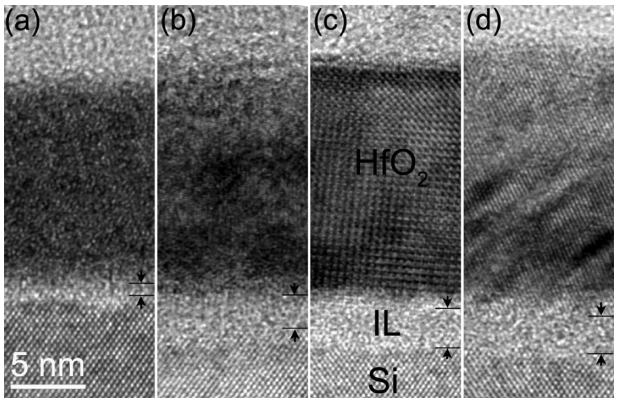

Figure 2. Cross-sectional HRTEM images of the sample (a) as-deposited, annealed in (b) N_2, (c) air, and (d) O_2.

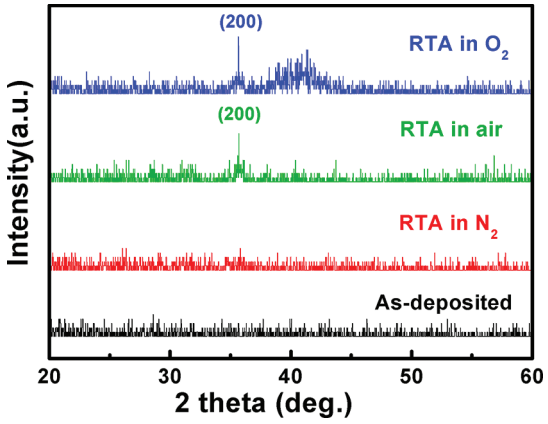

Figure 3. XRD patterns of the as-deposited and annealed samples.

The microstructure of the dielectric layer and the HfO_2/Si interface of the as-deposited and annealed samples have been investigated by cross-sectional HRTEM as shown in Figure 2. The as-deposited and N_2 annealed samples show an amorphous structure. However, monoclinic HfO_2 phase is identified in the samples annealed in air and O_2. These results are confirmed by XRD characterization, no obvious diffraction peak can be observed for the as-deposited sample as well as the sample annealed in the N_2, and a monoclinic phase (200) peak can be observed in the sample annealed in air and O_2, as showing in Figure 3. The thickness of the HfO_2 dielectric layer is determined as 14.2 ± 0.3 nm, 15.7 ± 0.4 nm, 17.6 ± 0.3 nm, and 16.1 ± 0.2 nm for the sample as-deposited, annealed in N_2, air, and O_2, respectively. For the as-deposited sample, the slight increase in the thickness of the dielectric layer after annealing may due to the crystallization and grain growth. The light contrast between the dielectric layer and substrate indicates an interfacial layer of 0.8 ± 0.1 nm formed during deposition. In contrast with our previous results,[17] the interfacial layer is much thinner than the sample deposited in oxygen. The mechanism of nitrogen suppressing the interfacial reaction is more or less similar with that in situ ionized nitrogen restricts the interfacial reaction, the nitrogen molecules quench the atomic vibration of Si atoms and reduce the probability of O atoms diffusion into the Si forming the interfacial layer.[18] Furthermore, comparison with the sample deposited in in situ ionized nitrogen,[18] the thicker interfacial layer may

Table 1. Extracted Parameters of MOS Capacitors

	C−V hysteresis (V)	V_{FB} from C−V (V)	Q_m ($\times 10^{10}$ cm^{-2})	Q ($\times 10^{12}$ cm^{-2})
as-deposited	0.054 ± 0.001	−1.05 ± 0.03	8.59 ± 0.16	2.65 ± 0.05
RTA in N_2	0.043 ± 0.001	−0.33 ± 0.02	7.17 ± 0.17	1.54 ± 0.03
RTA in air	0.016 ± 0.001	−0.26 ± 0.01	3.63 ± 0.23	1.95 ± 0.02
RTA in O_2	0.011 ± 0.001	0.21 ± 0.01	2.74 ± 0.25	1.01 ± 0.02

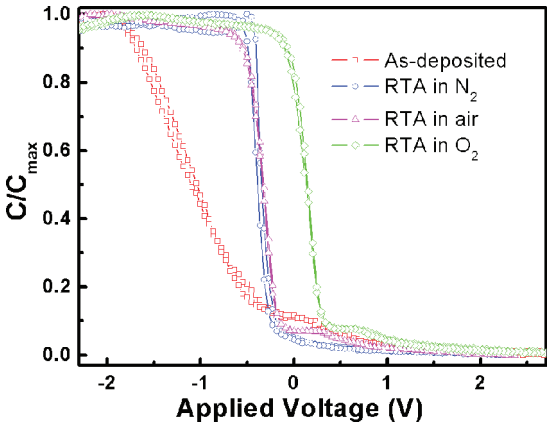

Figure 4. $C-V$ hysteresis of the as-deposited and annealed HfO_2 films at various conditions.

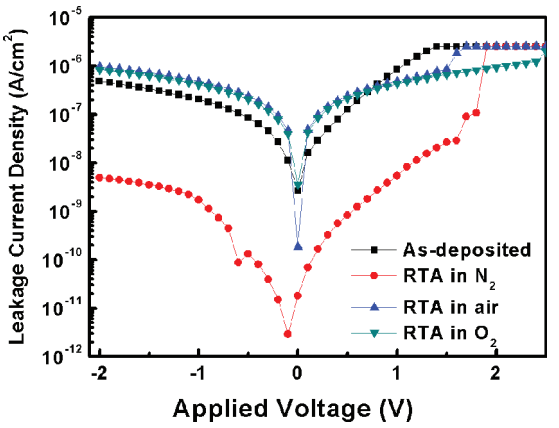

Figure 5. $J-V$ curves of the as-deposited and annealed HfO_2 films.

originate from the relative lower kinetic energy of the nitrogen than the ionized one.

After the RTA processing, the thickness of the interfacial layer increases substantially to 2.2 ± 0.1 nm, 2.6 ± 0.1 nm, and 2.5 ± 0.2 nm for annealed in N_2, air, and O_2, respectively. As reported by Miyata et al,[19] usually, there are two stages in the growth of the interfacial layer: the reaction of Si substrate with HfO_2 all through the deposition and the oxygen diffusion during the postannealing. In the relative inert ambient, the first stage is slow and the interfacial oxidation is suppressed. During the annealing, the HfO_2 film crystallized or partially crystallized and the crystallization of the HfO_2 initiated and speeded up the second stage,[19] which result in a sharp increase in the interfacial layer thickness. Busch et al[20] reported the fast interfacial oxidation in ZrO_2/Si interface based on oxygen diffusion at the crystalline boundary. These results shine an insight that suppressing the crystallization of the dielectric layer is useful for controlling the interfacial oxide.

3.2. Electrical Analyses of the Pt/HfO_2/Si MOS Devices. Normalized $C-V$ curves of the Pt/HfO_2/Si capacitors with various atmosphere annealed dielectric layers are shown in Figure 4. All the samples show a small C−V hysteresis, the $C-V$ hysteresis at half value of accumulation capacitance, the flat band voltage (V_{FB}), the mobile charges and the total charge in the MOS capacitors estimated from the curves are collected in Table 1. The flat band voltage (V_{FB}) extracted from the curves were −1.05 ± 0.03 V, −0.33 ± 0.02 V, −0.26 ± 0.01 V, and 0.21 ± 0.01 V for the HfO_2 films as-deposited, annealed in N_2, air and O_2 atmospheres, respectively. The negative V_{FB} value of the as-deposited sample reveals that the native defects/traps in the as-deposited sample are positive one: oxygen vacancy. In contrast with the sample as-deposited, the sample annealed shows a positive shift in V_{FB}, which indicates negative charge generation in the oxide or at the interface with Si during the annealing. The similar phenomenon has been reported elsewhere[10,21,22] and consists with our previous study.[17] The largest positive shift of the V_{FB} is observed in the sample annealed in O_2, about 1.26 V. The value of the shift is related to the increasing of the interface layer as well as the reduction of charge defect/trap density which is determined by capability of the compensating oxygen vacancies[23] and the neutralization of the interface trap charge during annealing,[24] as showing in Table 1.

Figure 5 shows the current density−voltage ($J-V$) characteristics of the as-deposited and annealed samples. It is clear that all the HfO_2 samples show lower leakage current than that of SiO_2 at the same EOT (1×10^{-6} A/cm^{-2} @ 1 V).[25] The leakage current density in our sample as-deposited and annealed in air and O_2 are at the same order in magnitude with atomic layer deposition grown HfO_2 in same dielectric thickness reported by Do et al.[26] Both air and O_2 annealed samples showed similar leakage current characteristics as shown in Figure 5, this suggests that the conduction mechanism and the interface properties for both samples are similar. The sample annealed in N_2 shows a significant low leakage current density, about 2 orders of magnitude smaller than those as-deposited, annealed in air, O_2. The reason for the decrease of the leakage current density may be due to the reduction of oxide charge density[27,28] and the interfacial defect density[6] during the annealing process in comparison with the as-deposited sample, as well as the amorphous structure, which is indicated by XRD and HRTEM in comparison with the sample annealed in air and O_2. As summarized in Table 1, the as-deposited sample shows higher bulk and interface defect density than other samples. It is generally accepted that the grain boundary could serve as high leakage path.

To understand the interfacial quality, we carried out further detailed study on the current transport mechanism for the Pt/HfO_2/Si devices. The analysis shows that all the devices exhibit a similar current transport mechanism: Pool−Frenkel emission, for the gate injection case (negative voltage on the top electrode).

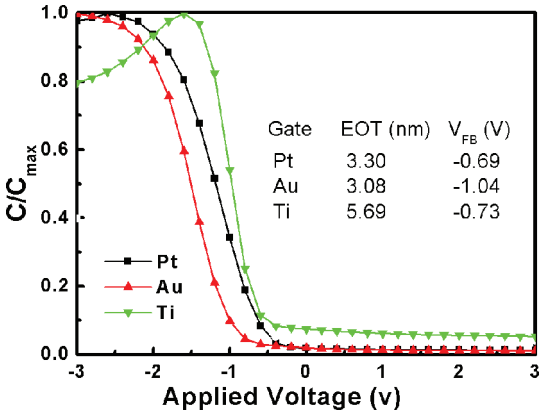

Figure 6. Capacitance−voltage curves of MOS capacitor with different metal gate. Inset table shows the extracted equivalent oxide thickness and flat band voltage for our three samples.

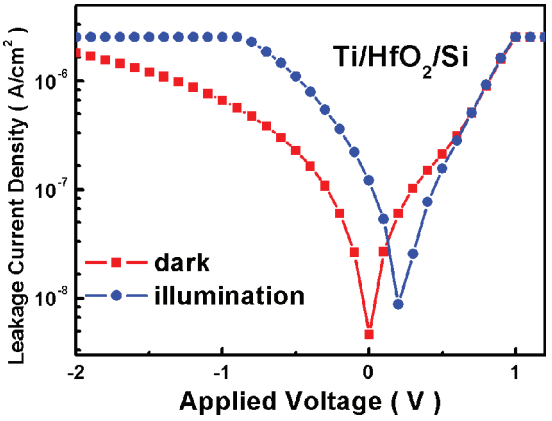

Figure 7. Typical plot of dark current and photocurrent for the Ti/HfO_2/Si devices.

For the substrate injection case (positive voltage on the top electrode), the current transport mechanism of device with dielectric layer as-deposited and annealed in N_2 are dominated by Pool−Frenkel emission. However, for the devices with dielectric layer annealed in air and O_2, the current is dominated by trap-assisted tunneling and Schottky emission. The difference in the carrier transport mechanism indicates that nitrogen has a beneficial effect on reducing the trap/defect density, and therefore significantly decreases the leakage current density.

3.3. Metal Electrode Effect on the Dielectric Properties of the HfO_2 Layer. In Figure 6, the normalized $C-V$ characteristic of the MOS capacitor with different metal gate (Pt, Au, and Ti) electrodes are presented. Considering the capacitors' gate area, the EOT and V_{FB} of each device were calculated, as presented in the inset table. From this table, we can clearly see that the EOT of the Ti-gated capacitor is the largest one, which could be attributed to possible parasitic parallel capacitances due to the formation of a rough top interface originating from the reaction between the gate electrode layer and the HfO_2 film.[29] This explanation can be verified by the photocurrent measurement result.

Figure 7 shows the $J-V$ curve of the Ti/HfO_2/Si devices with and without illumination. The device measured without illumination shows a lower leakage current than that with illumination

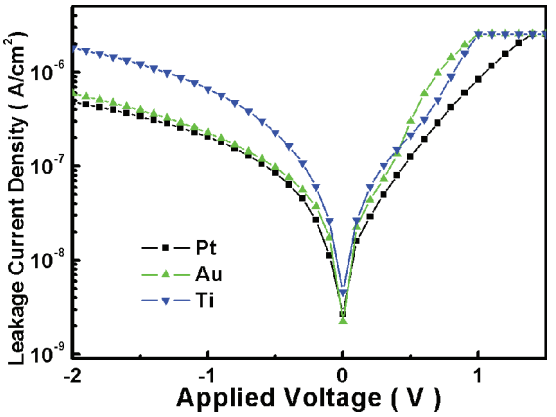

Figure 8. Leakage current density−voltage curves of MOS capacitor with different metal gate.

(A 150 W fiber optic lamp was used as the light source). The substantial increase in the leakage current from the dark to the photo flux is attributed to the internal photoemission of the carriers into the dielectric conduction band. The shift at negative gate voltage is much larger than at positive gate voltage, which implies that the centroid of the oxide charge is located closer to the gate than to the substrate,[30−32] which is consistent with the formation of parasitic interlayer between the Ti electrode and HfO_2.

As shown in the inset table in Figure 6, the devices with different gates have different V_{FB} values because of their different work functions as well as oxide charge density. The Au-gated device shows similar V_{FB} value reported by Atanassova et al.[33] The discrepancy in the V_{FB} for the Pt- and Au-gated capacitors is almost consistent with their work function difference. However, Ti-gated capacitor behaves differently. Taking into account their work function discrepancy, the oxide charges or traps located at the Ti/HfO_2 interface also plays an important role. Moreover, compare to the Pt gated device the right shift of the V_{FB} and increased EOT indicates the oxide charges or traps are mainly originated from the reaction of the Ti and HfO_2 during the electrode deposition. The interaction of the Ti gate and HfO_2 has also been reported by Goncharova et al.[34]

$J-V$ measurements were performed on several MOS capacitors for each sample and we only presented the most repeatable one. The Pt- and Au-gated devices show similar leakage current characteristics at the negative gate voltage as shown in Figure 8, may originate from similar leakage current conduction mechanism and interface properties for both samples. The Ti-gated capacitors show different leakage current characteristics with Pt and Au, which indicates that they have different conduction mechanisms and interface properties. This discrepancy may be due to the difference of their work function value, as shown in Figure 9d. To clarify this question, we need to discuss a detailed leakage current conduction mechanism.

To analyze the leakage current conduction mechanisms at the metal/HfO_2 interface, we have investigated many conduction mechanisms and evaluated the $J-V$ results at the gate injection (negative voltage on the top electrode) case. As show in panels a and b in Figure 9, under gate injections, the devices with Pt and Au electrodes fit the Pool−Frenkel emission mechanism very well. The large Pt (Au)/HfO_2 barrier height (for instance, about 2.48 eV for Pt/HfO_2), as well as the presence of trap energy band in the HfO_2, result in the Pool−Frenkel emission. Zhu et al.[35]

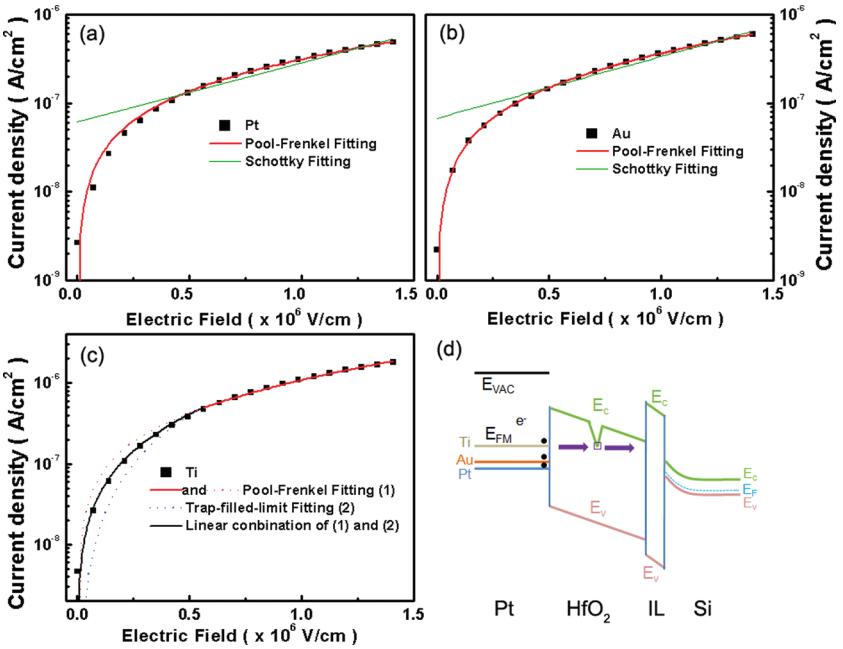

Figure 9. Conduction mechanisms fitting of MOS capacitor with different metal gate under gate injection. (a, b) Leakage current density under gate injection for the MOS devices with Pt and Au electrode and their Pool−Frenkel emission fitting. (c) Leakage current density for the device with Ti electrode and it is conduction mechanism fitting. (d) Schematic energy band diagram and the path of the Pool−Frenkel emission.

reported that the trap energy is about 1.5 eV below the conduction band of HfO_2 in the case of Pt/HfO_2, as shown in Figure 9d. However, for the device with Ti electrode, the situation is more complex. More specific, Pool−Frenkel emission dominates the conduction mechanism at higher electric field (>0.5 MV/cm), whereas below 0.5 MV/cm, the conduction mechanism is dominated by space-charge-limited conduction (trap-filled-limit emission) as well as Pool−Frenkel emission, as shown in Figure 9c. The presence of the space-charge limited conduction at low electric filed may be due to the small barrier height and charge traps located close to the Ti/HfO_2.

4. SUMMARY

The rapid thermal annealing influence on the structure, dielectric and electrical properties of the HfO_2 gate dielectric thin films was investigated. Because of dominated amorphous structure and reduced traps density, the sample annealed in N_2 shows the lowest leakage current. Capacitors with a high-k HfO_2 thin film as gate dielectric were fabricated, using three different metals for the top gate electrode: Pt, Au, and Ti. Capacitance−voltage and leakage current−voltage measurements show that the Pt- and Au-gated MOS devices have similar conduction mechanisms − Pool−Frenkel emission and interfacial properties at the metal/HfO_2 interface; by contrast, in the Ti-gated capacitor, the conduction mechanism is dominated by the linear combination of space-charge-limited conduction and Pool−Frenkel emission at low electric field and Pool−Frenkel emission at high field. The small barrier height of Ti/HfO_2 and charge traps result in the appearance of the space-charge-limited conduction at low electric field.

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REFERENCES

(1) Wilk, G. D.; Wallace, R. M.; Anthony, J. M. *J. Appl. Phys.* **2001**, *89*, 5243–5275.
(2) Lo, S. -H.; Buchanan, D. A.; Taur, Y.; Wang, W. *IEEE Electron Device Lett.* **1997**, *18*, 209–211.
(3) Robertson, J. *Eur. Phys. J. Appl. Phys.* **2004**, *28*, 265–292.
(4) Huang, S. W.; Hwu, J. G. *IEEE Trans. Electron Devices* **2004**, *51*, 1877–1882.
(5) Kang, L.; Lee, B. H.; Qi, W. J.; Jeon, Y.; Nieh, R.; Gopalan, S.; Onishi, K.; Lee, J. C. *IEEE Electron Device Lett.* **2000**, *21*, 181–183.
(6) Wang, H.; Wang, Y.; Feng, J.; Ye, C.; Wang, B. Y.; Wang, H. B.; Li, Q.; Jiang, Y.; Huang, A. P.; Xiao, Z. S. *Appl. Phys. A: Mater. Sci. Process.* **2008**, *93*, 681–684.
(7) Lin, C. P.; Tsui, B. Y.; Tang, M. J.; Huang, R. H.; Chien, C. H. *IEEE Electron Device Lett.* **2006**, *27*, 360–363.
(8) Onishi, K.; Kang, C. S.; Choi, R.; Kim, Y. H.; Krishnan, S.; Akbar, M. S.; Lee, J. C. *IEEE Electron Device Lett.* **2003**, *24*, 254–256.
(9) Callegri, A.; Cartier, E.; Gribelyuk, M.; Okorn-Schmidt, H. F.; Zabel, T. *J. Appl. Phys.* **2001**, *90*, 6466–6475.
(10) Kamel, F. E.; Gonon, P.; Vallee, C. *Appl. Phys. Lett.* **2007**, *91*, 172909.
(11) Kim, Y. M.; Lee, J. S. *Appl. Phys. Lett.* **2008**, *92*, 102901.
(12) Kamel, F. E.; Gonon, P.; Vallee, C.; Jorel, C. *J. Appl. Phys.* **2009**, *106*, 064508.
(13) Chau, R.; Datta, S.; Doczy, M.; Doyle, B.; Kavalieros, J.; Metz, M. *IEEE Electron Device Lett.* **2004**, *25*, 408–410.
(14) Wenger, Ch.; Lukosius, M.; Mussig, H. -J.; Ruhi, G.; Pasko, S.; Lohe, Ch. *J. Vac. Sci. Technol. B* **2009**, *27*, 286–289.

(15) Zhu, S. Y.; Yu, H. Y.; Whang, S. J.; Chen, J. H.; Shen, C.; Zhu, C.; Lee, S. J.; Li, M. F. *IEEE Electron Device Lett.* **2004**, *25*, 268–270.
(16) Wu, X.; Pey, K. L.; Zhang, G.; Bai, P.; Li, X.; Liu, W. H.; Raghavan, N. *Appl. Phys. Lett.* **2010**, *96*, 202903.
(17) Wang, H.; Wang, Y.; Zhang, J.; Ye, C.; Wang, H. B.; Feng, J.; Wang, B. Y.; Li, Q.; Jiang, Y. *Appl. Phys. Lett.* **2008**, *93*, 202904.
(18) Wang, Y.; Wang, H.; Zhang, J.; Wang, H. B.; Ye, C.; Jiang, Y.; Wang, Q. *Appl. Phys. Lett.* **2009**, *95*, 032905.
(19) Miyata, N. *Appl. Phys. Lett.* **2006**, *89*, 102903.
(20) Busch, B. W.; Schulte, W. H.; Garfunkel, E.; Gustafsson, T.; Qi, W.; Nieh, R.; Lee, J. *Phys.Rev.B* **2000**, *62*, R13290–R13293.
(21) Schaeffler, J. K.; Fonseca, L. R. C.; Samavedam, S. B.; Liang, Y.; Tobin, P. J.; White, B. E. *Appl. Phys. Lett.* **2004**, *85*, 1826–1828.
(22) Pereira, L.; Barquinha, P.; Fortunato, E.; Martins, R. *Mater. Sci. Semicond. Proc.* **2006**, *9*, 1125–1132.
(23) Kamada, H.; Tanimura, T.; Toyoda, S.; Kumigashira, H.; Oshima, M.; Liu, G. L.; Liu, Z.; Ikeda, K. *Appl. Phys. Lett.* **2008**, *93*, 212903.
(24) Lin, C.; Zhang, N. L.; Shen, Q. W. *Met. Mater. Int.* **2004**, *10*, 475.
(25) Lo, S.-H.; Buchanan, D. A.; Taur, Y.; Wang, W. *IEEE Electron Device Lett.* **1997**, *18*, 209.
(26) Do., S. W.; Lee, Y. H.; Lee, J. S. *J. Kor. Phys. Soc.* **2007**, *50*, 666.
(27) Umezawa, N.; Shiraishi, K.; Torii, K.; Boero, M.; Chikyow, T.; Watanabe, H.; Yamabe, K.; Ohno, T.; Yamada, K.; Nara, Y. *IEEE Electron Device Lett.* **2007**, *28*, 363–365.
(28) Shang, G.; Peacock, P. W.; Robertson, J. *Appl. Phys. Lett.* **2004**, *84*, 106–108.
(29) Cheng, X. H.; Wan, L.; Song, Z. R.; Yu, Y. H.; Shen, D. S. *Appl. Phys. Lett.* **2007**, *90*, 152910.
(30) Fleming, R. M.; Lang, D. V.; Jones, C. D. W.; Steigerwald, M. L.; Murphy, D. W.; Alers, G. B.; Wong, Y. -H.; van Dover, R. B.; Kwo, J. R.; Sergent, A. M. *J. Appl. Phys.* **2000**, *88*, 850–862.
(31) Felnhofer, D.; Gusev, E. P.; Jamison, P.; Buchanan, D. A. *Microelectron. Eng.* **2005**, *80*, 58–61.
(32) Felnhofer, D.; Gusev, E. P.; Jamison, P.; Buchanan, D. A. *J. Appl. Phys.* **2008**, *103*, 054101.
(33) Atanassova, E.; Paskaleva, A.; Novkovski, N. *Microelectron. Reliab.* **2008**, *48*, 514–525.
(34) Goncharova, L. V.; Dalponte, M.; Gustafsson, T.; Celik, O.; Garfunkel, E.; Lysaght, P. S.; Bersuker, G. *J. Vac. Sci. Technol. A* **2007**, *25*, 261–268.
(35) Zhu, W. J.; Ma, T. P.; Tanagawa, T.; Kim, J.; Di, Y. *IEEE Electron Device Lett.* **2002**, *23*, 97.